IN THE SPECIFICATION:

Please replace paragraph 16 of the specification with the following:

[0016] However, the claimed subject matter is not limited to two power states. For example, it supports more than two power states by allowing for each PLL to have different voltage and frequencies (which is discussed further in connection with Figure 3). As the frequency or voltage is changed, it might require a time penalty of [[4-5 us]] 4-5μs in one embodiment to allow for PLL relock.